LISTING OF CLAIMS

1. (Previously presented) A pixel cell, comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

2. (Original) The pixel cell of claim 1, wherein said photosensitive element is a photodiode.

3. (Original) The pixel cell of claim 1, wherein said first storage node comprises a gated storage node.

4. (Original) The pixel cell of claim 1, wherein said first storage node comprises a storage capacitor.

5. (Original) The pixel cell of claim 1, wherein said second storage node comprises a gated storage node.

6. (Original) The pixel cell of claim 1, wherein said second storage node comprises a storage capacitor.

7. (Original) The pixel cell of claim 3, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

8. (Original) The pixel cell of claim 7, wherein said depletion area and said barrier region comprise oppositely doped silicon.

9. (Original) The pixel cell of claim 1 further comprising a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

10. (Original) The pixel cell of claim 1 further comprising:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.

11. (Previously presented) A semiconductor chip, comprising:

a plurality of pixel cells, each of said plurality of pixel cells comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated during the integration period by said photosensitive element that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

12. (Original) The chip of claim 11, wherein said photosensitive element is a photodiode.

13. (Original) The chip of claim 11, wherein said first storage node comprises a gated storage node.

14. (Original) The chip of claim 11, wherein said first storage node comprises a storage capacitor.

15. (Original) The chip of claim 11, wherein said second storage node comprises a gated storage node.

16. (Original) The chip of claim 11, wherein said second storage node comprises a storage capacitor.

17. (Original) The chip of claim 13, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

18. (Original) The chip of claim 17, wherein said depletion area and said barrier region comprise oppositely doped silicon.

19. (Original) The chip of claim 11 further comprising a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

20. (Original) The chip of claim 11 further comprising:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.

21. (Original) The chip of claim 11 further comprising a sample and hold circuit for receiving said charge stored by said floating diffusion region.

22. (Original) The chip of claim 21, wherein said sample and hold circuit comprises at least four storage nodes, each respectively for storing a reset voltage and a signal voltage representing a charge stored by each of said first and second storage nodes.

23. (Original) The chip of claim 21, wherein said sample and hold circuit further comprises at least two storage nodes for respectively storing a reset voltage of said floating diffusion region and a signal voltage of at least one of said first and second storage nodes.

24. (Previously presented) A semiconductor chip, comprising:

a plurality of pixel cells, at least two of which share a common floating diffusion region, each of said at least two pixel cells further comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at said common floating diffusion region; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

25. (Previously presented) A method for operating an image sensor, the method comprising:

receiving, at a first storage node of a pixel cell, charge generated by a photosensitive element of said pixel cell during an integration period;

receiving, at a second storage node of said pixel cell, a portion of said charge generated by said photosensitive element during the integration period not stored at said first storage node; and

transferring said charge from at least one of said first and second storage nodes to a floating diffusion region of said pixel cell.

26. (Original) The method of claim 25, wherein said first act of receiving comprises receiving said charge at a gated storage node of said pixel cell.

27. (Original) The method of claim 25, wherein said second act of receiving comprises receiving said portion of said charge at a storage capacitor of said pixel cell.

28. (Original) The method of claim 25, wherein said act of transferring comprises:

transferring said charge from said first storage node to said floating diffusion region; and

transferring said charge from said floating diffusion region to a column line associated with said pixel cell.

29. (Original) The method of claim 25, wherein said act of transferring comprises:

transferring said charge from said second storage node to said floating diffusion region; and

transferring said charge from said floating diffusion region to a column line associated with said pixel cell.

30. (Original) The method of claim 25, wherein said first act of receiving comprises activating a shutter gate transistor coupled between said first storage node and said photosensitive element.

31. (Original) The method of claim 25, wherein said second act of receiving comprises activating a shutter gate transistor coupled between said second storage node and said photosensitive element.

32. (Original) The method of claim 25, wherein said act of transferring comprises activating a transfer transistor coupled between at least one of said first and second storage nodes and said floating diffusion region.

33. (Previously presented) A method for operating an image sensor, the method comprising:

receiving light at a photosensitive element of a first pixel cell during an integration period;

transferring charge generated during the integration period by said photosensitive element to a first storage node of said first pixel cell;

transferring a portion of said charge generated during the integration period not transferred to said first storage node to a second storage node of said first pixel cell;

transferring said charge from said first storage node to a floating diffusion region of said first pixel cell;

reading out said charge from said floating diffusion region;

transferring said charge from said second storage node to said floating diffusion region; and

reading out said charge from said floating diffusion region.

34. (Original) The method of claim 33 further comprising the act of resetting at least one of said photosensitive element and said floating diffusion region.

35. (Original) The method of claim 33 further comprising:

receiving light at a second photosensitive element of a second pixel cell;

transferring charge generated by said second photosensitive element to a first storage node of said second pixel cell;

transferring a portion of said charge not transferred to said first storage node of said second pixel cell to a second storage node of said second pixel cell;

transferring said charge from said first storage node of said second pixel cell to said floating diffusion region, wherein said first and second pixel cells share said floating diffusion region;

reading out said charge from said floating diffusion region;

transferring said charge from said second storage node of said second pixel cell to said floating diffusion region; and

reading out said charge from said floating diffusion region.

36. (Previously presented) A processor system, comprising:

a processor; and

an imager device coupled to said processor, said imager device having an array of pixel cells, each pixel cell comprising:

a first storage node for storing charge generated at a photosensitive element during an integration period prior to storing said charge at a floating diffusion region of said pixel cell; and

a second storage node for storing a portion of said charge generated by said photosensitive element during the integration period that is not stored by said first storage node and prior to storing said portion of said charge at said floating diffusion region.

37. (Original) The processor system of claim 36, wherein said photosensitive element is a photodiode.

38. (Original) The processor system of claim 36, wherein said first storage node comprises a gated storage node.

39. (Original) The processor system of claim 36, wherein said first storage node comprises a storage capacitor.

40. (Original) The processor system of claim 36, wherein said second storage node comprises a gated storage node.

41. (Original) The processor system of claim 36, wherein said second storage node comprises a storage capacitor.

42. (Original) The processor system of claim 38, wherein said gated storage node comprises:

a depletion area between said photosensitive element and said floating diffusion region; and

a barrier region adjacent to said depletion area.

43. (Original) The processor system of claim 42, wherein said depletion area and said barrier region comprise oppositely doped silicon.

44. (Original) The processor system of claim 36, wherein each pixel cell further comprises a first transfer transistor switchably coupled between at least one of said first and second storage nodes and said floating diffusion region.

45. (Original) The processor system claim 36, wherein each pixel cell further comprises:

a first transfer transistor switchably coupled between said first storage node and said floating diffusion region; and

a second transfer transistor switchably coupled between said second storage node and said floating diffusion region.